

**WHAT IS CLAIMED IS:**

1. A method of fabricating a semiconductor device comprising:
  - 5 forming an interconnection line over a substrate, wherein the interconnection line functions as a first electrode;
  - forming a first insulating layer on the substrate and the interconnection line;
  - 10 forming an electrode layer and an oxide layer on the first insulating layer;
  - 15 forming a photoresist pattern on the oxide layer;
  - etching the oxide layer and the electrode layer to form a second electrode and an oxide layer pattern stacked over the interconnection line, wherein at least the electrode layer is wet-etched; and
  - removing the photoresist pattern.
2. The method of claim 1, wherein the step of forming the interconnection line comprises:
  - forming a second insulating layer on the substrate; and
  - 20 forming a pattern in the second insulating layer using a damascene technique.
3. The method of claim 2, wherein the pattern is formed from a copper layer.

4. The method of claim 1, wherein the first insulating layer is formed of a dielectric layer.

5. The method of claim 4, wherein the dielectric layer is formed of one of a silicon nitride layer, a silicon carbide layer, a silicon oxycarbide layer and a silicon carbonitride layer.

10 6. The method of claim 1, wherein the electrode layer is formed of one of a tantalum layer, a tantalum nitride layer, a titanium layer and a titanium nitride layer.

15 7. The method of claim 1, wherein etching is performed using a mixture of hydrofluoric acid and nitric acid.

8. The method of claim 1, wherein the electrode layer is formed of one of a tungsten layer and a tungsten nitride layer.

20 9. The method of claim 1, wherein the oxide layer is one of wet-etched and dry-etched, and the electrode layer is wet-etched using hydrogen peroxide.

10. The method of claim 1, further comprising using the photoresist

pattern as an etching mask.

11. The method of claim 1, wherein the electrode layer is formed from metal.

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12. The method of claim 1, wherein the interconnection line is formed from metal.

10 13. A method of fabricating a semiconductor device comprising:  
forming an interconnection line over a substrate, wherein the  
interconnection line functions as a first electrode;  
forming an insulating layer on the substrate and the interconnection  
line;  
forming an electrode layer on the insulating layer;  
15 forming a photoresist pattern on the electrode layer; and  
wet-etching the electrode layer to form a second electrode.

20 14. The method of claim 13, wherein the interconnection line is formed from metal.

15. The method of claim 13, wherein the insulating layer is formed from a dielectric layer.

16. The method of claim 15, wherein the dielectric layer is formed of one of a silicon nitride layer, a silicon carbide layer, a silicon oxycarbide layer and a silicon carbonitride layer.

5 17. The method of claim 13, wherein the electrode layer is formed of one of a tantalum layer, a tantalum nitride layer, a titanium layer, a titanium nitride layer, a tungsten layer and a tungsten nitride layer.

10 18. The method of claim 13, wherein the electrode layer is wet-etched using one of hydrogen peroxide and a mixture of hydrofluoric acid and nitric acid.

15 19. The method of claim 13, further comprising:  
forming an oxide layer on the electrode layer; and  
one of wet-etching and dry-etching the oxide layer.

20. The method of claim 13, further comprising removing the photoresist pattern.

20 21. The method of claim 13, wherein the electrode layer is formed from metal.